REMARKS

The Final Office Action mailed September 1, 2005, has been received and reviewed. Claims 1, 4 through 13 and 16 through 25 are currently pending in the application. Claims 1, 4 through 13 and 16 through 25 stand rejected. Applicant proposes to amend claims 1, 6, 8, 11, 13, 17, 23 and 25, and respectfully requests reconsideration of the application as proposed to be amended herein.

35 U.S.C. § 102 Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 6,389,490 to Camilleri et al.

Claims 11 and 12 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Camilleri et al. (U.S. Patent No. 6,389,490). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicant submits that the Camilleri reference does not and cannot anticipate under 35 U.S.C. § 102 the presently claimed invention of independent claim 11, and claim 12 depending therefrom, because the Camilleri reference does not describe, either expressly or inherently, the identical inventions in as complete detail as are contained in the claims.

The Office Action alleges:

> As per claim 11, Camilleri et al. teaches, with reference to figures 1 and 2, a FIFO buffer 101, a write address register 220 ("write counter") and a read address register 210 ("read counter"). The read address register includes a ***"last read address register" 216 ("at lest one pointer register configured to maintain a previous read counter setting*** and a "current read address register: 214 ("during a current reading from the FIFO"). (Office Action, pp. 3-4; emphasis added).

Applicant respectfully disagrees that the Camilleri reference anticipates Applicant's invention as claimed in independent claim 11 which reads:

> 11. A semiconductor substrate including a FIFO buffer, comprising:
> at least one FIFO;
> at least one write counter associated with the at least one FIFO; and
> at least one read counter associated with the at least one FIFO, the at least one read counter comprising ***at least one pointer register configured to maintain a previous read counter setting of the at least one read counter as a current reading location of the FIFO.*** (Emphasis added.)

In contrast, the Camilleri reference utilizes the last read address register circuit for determining the status of a buffer rather than for utilization as a reading location. Specifically the Camilleri reference discloses:

> FIFO memory system includ[ing] a memory, a write address counter, a read address counter, a flag control circuit for generating FUL and EMPTY command signals, ... (Camilleri, col. 3, lines 26-28).
>
> Full control signal is generated when the current binary write address is one memory location behind the current binary read address, thereby preventing the write address counter form "catching up" to the read address counter[]. (Camilleri, col. 3, lines 14-18).
>
> FIFO memory system 100 includes . . . dual-port FIFO RAM . . ., . . . write address counter . . ., . . . read address counter . . ., a flag control circuit 107, ... (Camilleri, col. 5, lines 4-9).
>
> Flag control circuit 107 is generally divided into a read address register section 210, a write address register section 220, and a comparator circuit 230. (Camilleri, col. 7, lines 10-12).
>
> Read address register section 210 includes a binary-to-Gray-code converter 212, a current read address register circuit 214, and a last read address register circuit 216. (Camilleri, col. 7, lines 15-18).
>
> [L]ast read address register circuit 216 receives the current read address value [] and, . . . stores this data . . . that is transmitted to comparator circuit 230. (Camilleri, col. 7, lines 35-40).
>
> Comparator circuit 230 receives the . . . read address values from read address register section 210, . . . and generates the FULL and EMPTY control signals when predetermined conditions are met by these signals. (Camilleri, col. 7 line 66 through col. 8, line 5).

Clearly, the Camilleri reference discloses a "last read address register circuit 216 [that] receives the current read address value [] and, . . . stores this data . . . that is transmitted [and] generates [] FULL and EMPTY control signals". (Camilleri, col. 7, line 35 through col. 8, line 4). However, nothing in the Camilleri reference discloses ***"at least one pointer register configured to maintain a previous read counter setting of the at least one read counter as a current reading location of the FIFO"*** as claimed by Applicant in presently amended independent claim 11.

Therefore, presently amended independent claim 1, and claim 12 depending therefrom, are not anticipated by the Camilleri reference under 35 U.S.C. § 102. Accordingly, such claims are allowable over the cited prior art and Applicant respectfully requests that such rejections be withdrawn.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,487,049 to Hang in view of U.S. Patent No. 6,389,490 to Camilleri et al.

Claims 1, 4, 6, and 17-25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hang (U.S. Patent No. 5,487,049) in view of Camilleri et al. (U.S. Patent No. 6,389,490). Applicant respectfully traverses this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 1, 4, 6, and 17-25 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claims limitations.

Applicants sustain the above-proffered arguments that neither the Hang reference nor the Camilleri reference, either individually, or in any proper combination, teach or suggest Applicant's invention as claimed in presently amended independent claims 1, 6, 17, 23 and 25.

Claims 1 and 4

The Office Action introduces the Hang reference and alleges:

> As per claim 1, . . . Hang does not teach "at least one read counter associated with the FIFO and configured to maintain a previous read counter setting of the read conter during a current reading form the FIFO".
>
> Camilleri et al. teaches, with reference to figures 1 and 2, a FIFO buffer 101 and a read address register 210 ("read counter"), where the read address register includes a "last read address register" 216 ("at least one pointer register configured to maintain a previous read counter setting") and a "current read address register" 214 ("during a current reading from the FIFO"). See also column 7, lines 32-43. In order to determine whether the [] buffer is full, the write counter value is compared to the last used ("previous") read counter value (column 3, line 65-67), as opposed to the prior art described by Camilleri et al. (and similar to the system of Hang et al.), where in order to determine if a buffer is full, the write counter is compared to the current read counter value. (Office Action, pp. 3-4).

Applicant sustains the above-proffered arguments regarding the teachings and suggestion of the Camilleri reference as well as the Office Action's admissions of the deficient teaching and suggestion of the Hang reference. Applicant respectfully submits that neither of the cited references, namely the Hang reference and the Camilleri reference, either individually or in any proper combination, teach or suggest Applicant's invention as presently claimed, namely:

> 1. A dynamic random access memory device (DRAM), comprising:
> at least one memory bank;
> control logic associated with the at least one memory bank to control data corresponding to a memory command within the DRAM; and
> a FIFO associated with the control logic, the FIFO configured for temporarily storing at least one memory command until at least one of the data corresponding to the at

> least one memory command arrives at the DRAM, the at least one memory command including an address within the at least one memory, the control logic further configured for simultaneous reading and writing from the FIFO, the control logic further including ***at least one read counter*** associated with the FIFO and ***configured to maintain a previous read counter setting of the read counter as a current reading location of the FIFO.*** (Emphasis added.)

Therefore, Applicant respectfully requests that the rejection of presently amended independent claim 1, and claim 4 depending therefrom, be withdrawn.

Claim 6

The Office Action introduces the Hang reference and alleges:

> As per claim 6, Hang teaches a FIFO system 10 including a FIFO data buffer 30 and address buffer 34, a write counter 22, and a read counter 26. See figure 1. The claim is further rejected for the reasons set forth for claim 1, above. (Office Action, p. 4).

Applicant sustains the above-proffered arguments regarding the teachings and suggestion of the Camilleri reference as well as the Office Action's admissions of the deficient teaching and suggestion of the Hang reference. Applicant respectfully submits that neither of the cited references, namely the Hang reference and the Camilleri reference, either individually or in any proper combination, teach or suggest Applicant's invention as presently claimed, namely:

> 6. A FIFO buffer system in a dynamic random access memory device (DRAM), comprising:
> a FIFO configured for temporarily storing at least one memory command until at least one data corresponding to the at least one memory command arrives at the DRAM;
> at least one write counter associated with the FIFO; and
> at least one read counter associated with the FIFO, the ***at least one read counter*** comprising at least one pointer register ***configured to maintain a previous read counter setting of the at least one read counter as a current reading location of the FIFO.*** (Emphasis added.)

Therefore, Applicant respectfully requests that the rejection of presently amended independent claim 6, and claim 7 depending therefrom, be withdrawn.

Claims 17 through 22

The Office Action introduces the Hang reference and alleges:

> As per claim 17, . . . [t]he claim is further rejected for the reasons set forth above for claim 1. (Office Action, pp. 4-5).

Applicant sustains the above-proffered arguments regarding the teachings and suggestion of the Camilleri reference as well as the Office Action's admissions of the deficient teaching and suggestion of the Hang reference. Applicant respectfully submits that neither of the cited references, namely the Hang reference and the Camilleri reference, either individually or in any proper combination, teach or suggest Applicant's invention as presently claimed, namely:

> 17. A method of storing data in a DRAM, comprising:
> providing a DRAM comprising at least one memory bank, control logic associated with the at least one memory bank, and a FIFO associated with the control logic, the FIFO configured for temporarily storing a memory bank address command until data corresponding to the memory bank address command arrives at the DRAM, the at least one memory command specifying addressing within the at least one memory bank, the control logic configured for simultaneous reading and writing from the FIFO, the control logic further including ***a read counter*** associated with the FIFO and ***configured to maintain a previous read counter setting of the read counter as a current reading location of the FIFO;***
> receiving the memory bank address command at the control logic;
> writing the memory bank address command to the FIFO;
> receiving data corresponding to the memory bank address command at the control logic;
> reading the memory bank address command from the FIFO; and
> storing the data at a memory bank address indicated by the memory bank address command. (Emphasis added.)

Therefore, Applicant respectfully requests that the rejection of presently amended independent claim 17, and claims 18 through 22 depending therefrom, be withdrawn.

Claims 23 and 24

The Office Action introduces the Hang reference and alleges:

> As per claim 23, . . . [t]he claim is further rejected for the reasons set forth above for claim 1. (Office Action, p. 6).

Applicant sustains the above-proffered arguments regarding the teachings and suggestion of the Camilleri reference as well as the Office Action's admissions of the deficient teaching and suggestion of the Hang reference. Applicant respectfully submits that neither of the cited references, namely the Hang reference and the Camilleri reference, either individually or in any proper combination, teach or suggest Applicant's invention as presently claimed, namely:

> 23. A method of buffering a data stream including a memory bank address command and data corresponding to the memory bank address command in an electronic device, the method comprising:
> providing a FIFO buffer system having a read counter pointing at a first buffer of a FIFO including a series of FIFO buffers and a write counter pointing at the first buffer of the FIFO, the FIFO buffers configured for temporarily storing the memory bank address command while retrieving the data corresponding to the memory bank address command;
> receiving the memory bank address command of the data stream at the FIFO buffer system;
> storing the memory bank address command of the data stream in the first buffer of the FIFO;
> adjusting the write counter to point at a second buffer in the series of FIFO buffers; and
> maintaining the write counter pointing to at least one FIFO buffer, in the series of FIFO buffers, ahead of the first buffer at which the read counter is pointing and maintaining ***the read counter pointing to at least one FIFO buffer associated with a previous read counter setting of the read counter as a current reading location of the FIFO.*** (Emphasis added.)

Therefore, Applicant respectfully requests that the rejection of presently amended independent claim 23, and claim 24 depending therefrom, be withdrawn.

Claim 25

The Office Action introduces the Hang reference and alleges:

> As per claim 25, . . . [t]he claim is further rejected for the reasons set forth for claim 1, above. (Office Action, p. 6).

Applicant sustains the above-proffered arguments regarding the teachings and suggestion of the Camilleri reference as well as the Office Action's admissions of the deficient teaching and suggestion of the Hang reference. Applicant respectfully submits that neither of the cited

references, namely the Hang reference and the Camilleri reference, either individually or in any proper combination, teach or suggest Applicant's invention as presently claimed, namely:

> 25. A method of operating a memory device, the method comprising:
> receiving at least one memory bank address command;
> temporarily storing in a FIFO a first of the at least one memory bank address command, the FIFO including a series of FIFO buffers;
> temporarily storing in the FIFO a second of the at least one memory bank address command;
> receiving data corresponding to the first of the at least one memory bank address command;
> storing in the FIFO the data corresponding to the first of the at least one memory bank address command in response to the first of the at least one memory bank address command;
> receiving data corresponding to the second of the at least one memory bank address command; storing in the FIFO the data corresponding to the second of the at least one memory bank address command; and
> maintaining a write counter pointing to at least one FIFO buffer, in the series of FIFO buffers, ahead of a first FIFO buffer at which a read counter is pointing and maintaining ***the read counter pointing to at least another FIFO buffer associated with a previous read counter setting of the read counter as a current reading location of the FIFO.*** (Emphasis added.)

Therefore, Applicant respectfully requests that the rejection of presently amended independent claim 25 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,487,049 to Hang in view of U.S. Patent No. 6,389,490 to Camilleri et al. and further in view of U.S. Patent No. 5,699,530 to Rust et al.

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hang (U.S. Patent No. 5,487,049) in view of Camilleri et al.(U.S. Patent No. 6,389,490) and further in view of Rust et al. (U.S. Patent No. 5,699,530). Applicant respectfully traverses this rejection, as hereinafter set forth.

The nonobviousness of independent claim 6 precludes a rejection of claim 7 which depends therefrom because a dependent claim is obvious only if the independent claim from which it depends is obvious. *See* In re Fine, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988), *see also*

MPEP § 2143.03. Therefore, the Applicant requests that the Examiner withdraw the 35 U.S.C. § 103(a) obviousness rejection to independent claim 6 and claim 7 which depends therefrom.

Obviousness Rejection Based on U.S. Patent No. 5,487,049 to Hang in view of U.S. Patent No. 6,389,490 to Camilleri et al. and further in view of U.S. Patent No. 5,289,584 to Thome et al.

Claims 8 through 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hang (U.S. Patent No. 5,487,049) in view of Camilleri et al.(U.S. Patent No. 6,389,490) and further in view of Thome et al.(U.S. Patent No. 5,289,584). Applicant respectfully traverses this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 8 through 10 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claims limitations.

Applicants sustain the above-proffered arguments that neither the Hang reference nor the Camilleri reference nor the Thome reference, either individually, or in any proper combination, teach or suggest Applicant's invention as claimed in presently amended independent claim 8 and claims 9 and 10 depending therefrom.

The Office Action introduces the Thome reference and alleges:

> As per claims 8 and 10, the claims are rejected for the reasons set forth for claim 6, above, further noting:
>
> Hang does not specifically mention a processor, input device (e.g. keyboard or mouse), output device (e.g. monitor), and a storage device (e.g. disk drive, tape drive). Thome et al. teaches a system including a page mode DRAM and a FIFO 114 or 116 (figure 2), which includes a CPU 30, keyboard 80 ("input device"), monitor 64 ("output device") and a hard disk 98 ("storage device"). (Office Action, p. 7).

Applicant sustains the above-proffered arguments regarding the teachings and suggestion of the Camilleri reference as well as the Office Action's admissions of the deficient teaching and suggestion of the Hang reference. Applicant respectfully submits that neither of the cited references, namely the Hang reference and the Camilleri reference and the Thome reference, either individually or in any proper combination, teach or suggest Applicant's invention as presently claimed, namely:

> 8. An electronic system, comprising:
> a processor;
> at least one of an input device, an output device and a storage device associated with the processor; and
> a memory device coupled to the processor for storing data and instructions for use by the processor, the memory device comprising:
> at least one FIFO configured for temporarily storing at least one of the instructions until at least one of the data corresponding to the at least one of the instructions arrives at the memory device;
> at least one write counter associated with the at least one FIFO; and
> at least one read counter associated with the at least one FIFO, the at least one read counter comprising at least one pointer register configured to maintain a previous read counter setting of the at least one read counter as a current reading location of the FIFO. (Emphasis added.)

Therefore, Applicant respectfully requests that the rejections of presently amended independent claim 8, and claims 9 and 10 depending therefrom, be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,487,049 to Hang in view of U.S. Patent No. 6,389,490 to Camilleri et al. and further in view of U.S. Patent No. 6,329,997 to Wu et al.

Claims 13 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hang (U.S. Patent No. 5,487,049) in view of Camilleri et al.(U.S. Patent No. 6,389,490) and further in view of Wu et al. (U.S. Patent No. 6,329,997). Applicant respectfully traverses this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 13 and 16 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claims limitations.

Applicants sustain the above-proffered arguments that neither the Hang reference nor the Camilleri reference nor the Wu reference, either individually, or in any proper combination, teach or suggest Applicant's invention as claimed in presently amended independent claim 13 and claim 16 depending therefrom.

> The Office Action introduces the Wu reference and alleges:
>
> As per claims 13 and 16, the combination of Hang and Camilleri et al. teaches the invention as set forth above for claim 1. However, Hang does not teach that the FIFO is embodied on a semiconductor structure (semiconductor wafer) with the DRAM. Wu et al. teaches that it was known to incorporate a FIFO on the same substrate with a DRAM. (Office Action, p. 8).

Applicant sustains the above-proffered arguments regarding the teachings and suggestion of the Camilleri reference as well as the Office Action's admissions of the deficient teaching and suggestion of the Hang reference. Applicant respectfully submits that neither of the cited references, namely the Hang reference and the Camilleri reference and the Wu reference, either individually or in any proper combination, teach or suggest Applicant's invention as presently claimed, namely:

> 13. A semiconductor substrate including a DRAM, comprising:
> at least one memory bank;
> control logic associated with the at least one memory bank to control at least one of data and commands within the DRAM; and
> a FIFO associated with the control logic, the FIFO configured for temporarily storing a memory command until data corresponding to the memory command arrives at the DRAM, the control logic further configured for simultaneous reading and writing of the at least one of data and commands from the FIFO, the control logic further including at least one read counter associated with the FIFO and configured to maintain a previous read counter setting of the read counter as a current reading location of the FIFO. (Emphasis added.)

Therefore, Applicant respectfully requests that the rejections of presently amended independent claim 13, and claim 16 depending therefrom, be withdrawn.

ENTRY OF AMENDMENTS

The proposed amendments to claims 1, 6, 8, 11, 13, 17, 23 and 25 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1, 4-13, 16-25 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,

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